WHAT IS CLAIMED IS:

1. A system for validating error detection logic, such system comprising:

a plurality of information paths, each one of such paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

a test word buffer for receiving a test word, such test word indicating a particular one of the plurality of information bits in a particular one of the information paths to be corrupted;

a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated the error detection logic, each one of such fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects such injected fault

2. The system recited in claim 1 wherein the test word buffer stores an indication as to whether software a processor used to control information flow through the logic is to be tested for response to a detected fault.

3. A method for testing error detection logic in a system, such system having a plurality of directors each adapted to handle a data transfer through logic in such system in accordance with software in such director, such software being adapted to deviate from a normal mode of operation in response to a report of a detected fault by such error detection logic, such method comprising:

establishing in the logic a condition for injecting a faults into the logic and indicating to such logic whether the fault is anticipated by a designated the one of the directors handling the transfer or unanticipated by such designated one of the data transfer handling director;

detecting when the designated one of the directors is handling a data transfer and in response to such detection injecting a fault into the logic, such injected fauklt being unanticipated by the designated director;

observing whether software in the designated one of the directors responds properly to the injected fault.

4. A method for validating error detection logic in a system, such method comprising:

designating a particular one of a plurality of directors to be tested for faults in software stored in such one of the directors, each one of the directors being adapted to feed information to the logic, such software being adapted to deviate from a normal operating process in response to detection of a fault reported to such director from the logic in such logic processing information fed thereto by such directors;

designating in such logic the particular one of the plurality of directors to be tested;

detecting when the designated one of the directors is feeding data to the logic;

injecting a fault into such logic upon such detection.

5. A method for validating error detection logic in a system, such method comprising:

testing whether hardware fault detection logic in the system are responding properly to hardware injected faults;

testing whether software in a designated one of a plurality of directors in such system responds properly to faults injected into the system with such designated director being *a priori* unaware of the injection of such fault.

6. A method for validating error detection logic in a system, such method comprising:

first testing whether hardware fault detection logics in the system are responding properly to hardware injected faults;

designating a particular one of a plurality of processors to be tested for faults in software stored in such processors, each one of the processors being adapted to feed information to the logic, such software being adapted to deviate from a normal operating process in response to detection of a fault reported to such director from the logic in such logic processing information fed thereto by such directors;

subsequent to the first test:

(a) designating in such logic the particular one of the plurality of processors to be tested;

(b) detecting when the designated one of the processors is feeding data to the logic; and

(c) injecting a fault into such logic upon such detection.

7. A data storage system wherein data is transferred between a host computer and a bank of disk drives through an interface, such interface having a plurality of front end directors coupled to the host computer and a plurality of back end directors coupled to the bank of disk drives, such data passing through a cache memory as such transferred data passes between the front end directors and the back end directors, such cache memory having control logic coupled between a memory region of the cache memory and the directors, such system having one of the directors adapted to send test words to the control logic, such control logic comprising:

a plurality of information paths, each one of such paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

a test word buffer for receiving the test words, such test words indicating:

a particular one of the plurality of information bits in a particular one of the information paths to be corrupted; and

whether a hardware test is to be performed on the error detection logic of the control logic or whether a software test is to be performed on the software in a designated one of the directors;

a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated one of the error detection logics, each one of such fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects such injected fault, such associated error detection logic reporting detection of faults to the one of the directors sending the test words when either the hardware test is to be performed or whether the software test on the designated one of the directors.

8. A data storage system wherein data is transferred between a host computer and a bank of disk drives through an interface, such interface having a plurality of front end directors coupled to the host computer and a plurality of back end directors coupled to the bank of disk drives, such data passing through a cache memory as such transferred data passes between

the front end directors and the back end directors, such front end and back end directors being coupled to the cache memory, such data being transferred as a series of transfers, each one of the transfers having associated therewith a tag, such tag having a plurality of fields, such fields identifying: the one of the directors to effect the transfer;; a memory location in the cache memory to store the data being transferred as such data is transferred through the interface; and, a random number unique in time to the transfer; such memory having control logic for controlling operation of the memory, respectively, such control logic being coupled between a memory region of the memory and the directors, such system having one of the directors adapted to send test words to the control logic, such control logic comprising:

a plurality of information paths, each one of such paths having associated therewith an error detection logic, each one of the paths having a plurality of information bits;

a test word buffer for receiving the test words, such test words indicating:

a particular one of the plurality of information bits in a particular one of the information paths to be corrupted;

whether a hardware test is to be performed on the control logic error detection logic or whether a software test is to be performed on the software in a handling one of the directors; and

wherein such test word has: a tag data portion and a tag mask portion, such tag mask portion being adapted to mask a selected one or ones of bits in the fields in a tag of a handling one of the directors;

a plurality of fault injectors responsive to the test word received by the buffer, each one of the fault injectors being disposed in a corresponding one of the information paths prior to the associated the error detection logic, each one of such fault injectors corrupting a selected one of the information bits in the corresponding one of the information paths in response to the test word received by the buffer to test whether the associated error detection logic detects such injected fault, such associated error detection logic reporting detection of faults to the one of the directors sending the test words when either the hardware test is to be performed or whether the software test is to be performed on the handling director when such handling director issuing a tag which when masked by the tag mask portion provides a tag masked portion indicated by the data tag received by the test buffer.

9. The system recited in claim 8 wherein the test word includes an indication of when the fault is to be injected into the fault injector after the initiation of a transfer and the time duration of such injected fault.

10. The system recited in claim 7 wherein the test word includes an indication of when the fault is to be injected into the fault injector after the initiation of a transfer and the time duration of such injected fault.